HAN

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,994	08/29/2003	Toshiaki Kirihata	FIS920030119US1	1993

32074 7590 03/02/2005

INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

EXAMINER	
YOHA, CONNIE C	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 03/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,994	KIRIHATA ET AL.	
	Examiner	Art Unit	
	Connie C. Yoha	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) *14-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Connie Yoha

CONNIE C. YOHA
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18 are presented for examination.

Claim Rejections - 35 USC ∋ 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Longway et al, Pat. No. 5563834.

With regard to claim 1, Longway discloses a memory array that simultaneously reads and writes different addresses of the same memory array (col. 5, line 40-42), comprising; a plurality of memory cells arranged in two equally sized arrays (fig. 4a, Upper Rom, and Lower Rom) having a separate read and write port (fig. 12) (col. 5, line 34-57), wherein each port is coupled to a wordline (fig. 12, Row1, Row2) that activates the memory cells, and a bitline that transfers data to or from said memory cells (fig. 12, BITLINE 1, BITLINE 1#) (col. 5, line 46-47); read wordlines and write wordlines respectively connected to the read and write ports of each memory cell along a row of each of said arrays (col. Line 42-57); a row of differential sense amplifiers (fig. 3a, 330) wherein one sense (fig. 4a, 330) is provided for each column of said array, and wherein each bitline from the first array being respectively attached to a first input terminal of the corresponding differential sense amplifier (fig. 4a, data line in the Upper ROM 301

connect to positive terminal of sense amplifier 330), and each read bitline from the second array being respectively attached to a second input terminal of the corresponding differential sense amplifier (fig. 4a, data line in the Lower Rom 302 connected to the negative terminal of sense amplifier 330); and a row of reference cells (fig. 4a, 451, 452) in each of said two arrays connected to a reference wordline (fig. 4a, REFEN, REFEN#) and the read bitlines, wherein when the reference wordline is activated, the read bitline coupled to the activated reference cell discharges to a voltage level that is mid-way the value at which a cell stores a logic 0 and a logic 1 (col. 3, line 18-25) (col. 3, line 62-col. 4, line 9).

With regard to claim 2, Longway discloses wherein each write bitline in the first array is connected to the write bitline in the second array in the same column (fig. 25 or 26), enabling simultaneous read and write by activating the read wordlines from the first array, the reference wordline from the second array, the write wordline from either the first or the second array and the write bitlines traversing both arrays, said arrangement resulting in transforming noise coupling from the write bitline to the read bitline into common mode noise that is rejected by said differential sense amplifiers (fig. 28) (col. 8, line 33-col. 9, line 17).

With regard to claim 3, Longway discloses wherein a write bitline in the first array and in the second array are respectively driven by a first and second driver (fig. 4a, 411, 412) having the same slew characteristics, said first and second drivers switching simultaneously (col. 4, line 62-67) (also with regard to claim 13).

With regard to claim 4 and 12, Longway discloses a memory array of memory cells, each cell provided with separate read and write ports (col. 5, line 40-42), comprising: read and write wordlines (fig. 12, Row 1, Row 2) coupling memory cells along each row of the array, read bitlines and write bitlines (fig. 12, BITLINE 1, BITLINE 1#) coupling cells along each column of the array, and differential read sense amplifiers (fig. 3a, 330) (col. 5, line 34-57); a read bitline pair with one read line connecting one terminal of a differential sense amplifier to a first half of the cells along a column of the array, and a second read bitline connecting the second half of the cells along the same column of the array (fig. 25, fig. 26); a first row of reference cells (fig. 4a, 451) connected to the first read bitline segments, and a second row of reference cells (fig. 4a, 452) connected to the second bitline segments; a first segment of a re-entrant read bitline linking a complementary input of the differential sense amplifier to a segment of the read bitline for each column; and a second segment of the re-entrant read bitline linking the second segment of the re-entrant read bitline linking the second segment of the read bitline and extending over the first section of the array arranged symmetrically about a horizontal line at the center of the array to the second segment of the re-entrant bitline (fig. 25 and fig. 26, fig. 27), wherein a simultaneous read and write operation is achieved by activating a read wordline in the first second of the array connected to the first bitline segment, a reference word line in the second portion of the array, a write wordline in the first or the second section of the array and all the write bitlines and all the differential sense amplifiers, and wherein a voltage swing on the write bitline couples an equivalent noise into all read bitline segments (fig. 25, fig. 26), thus

transforming the noise into a common mode noise which is detected and rejected by the differential sense amplifiers (col. 8, line 15-col. 9, line 17).

With regard to claim 5, Longway discloses wherein said first and second sections of the array have each the first and the second segments of said re-entrant read bitlines for each column of memory array (fig. 27) (col. 8, line 51-55) (also with regard to claim 8-11).

With regard to claim 6, Longway discloses wherein the write bitlines are driven by a row of write bitline drivers (fig. 4a, 411, 412) (col. 4, line 62-65) located along the periphery of the array (also with regard to claim 7).

Allowable Subject Matter

3. Claim 14-18 are objected as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record does not show the limitation of a memory array having in combination with other features, the re-entrant connection link one of the write drivers to a farther write bitline segment, and the write bitline drivers operating for each column in a way that the output voltage of the first driver is of the same magnitude and 180 degree out-of-phase from the output voltage of the second driver, and wherein when the voltage on the write bitline changes, no noise is coupled from the write bitlines to the read bitlines.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Wordeman et al (6845059), Shiratake et al (5418750), Lee et al (6570781) and Hosotani et al (5652728) disclose a memory device.

5. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

6. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1799. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, Hoai Ho, can be reached at (571) 272-1777. The fax phone number for this Group is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov should you

have questions on access to the Private Pair system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. Yoha

February 2005

CONNIE C. YOHA
PRIMARY EXAMINER